Md Yekra Rahman

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Summary

- **Available for Summer 2026 Internship in Analog IC Design.**
- Experienced in transistor-level design of op-amps, LDOs, bandgap references, charge-pumps, differential amplifiers and gate driver - level shifter circuits using Cadence Virtuoso using gm/ID methodology.
- Skilled in block validation, presentations and documentation.

Education

PhD Student in Electrical Engineering — Fall 2025 – Present
University of Missouri - Columbia, MO, USA

PhD Student in Electrical Engineering, Concentration: Circuits — Fall 2024 – Summer 2025
TxACE, University of Texas at Dallas, Richardson, TX, USA — GPA: 3.83/ 4.00

B.Sc. in Electrical and Electronic Engineering, Major : Electronics — April 2018 – May 2023
Bangladesh University of Engineering and Technology (BUET), Dhaka, Bangladesh — GPA: 3.65/ 4.00

Skills

IC Design Tools: Cadence Virtuoso, layout familiarity (DRC/LVS, parasitic extraction), LTSpice
Lab & Validation Equipment/Software: Oscilloscope, Network Analyzer, Signal Generator, SKILL, MATLAB

Research Experience

Projects — Fall 2024 – Present

Design of an Operational Amplifier using IBM 130 nm CMOS technology

- Designed a two-stage, Miller-compensated CMOS op-amp in IBM 130 nm using a small-signal and gm/ID-driven flow; sized in transistor-level and the layout aware compensation network to meet unity-gain bandwidth and phase-margin targets under a specified load and single-supply constraint.
- Validated performance with dedicated testbenches for open-loop gain/GBW/PM, slew rate, output swing, CMRR, and power, ensuring all transistors remained in saturation and complying with the single ideal current-source requirement.

DC–DC Buck Converter Design using TSMC 180 nm HV BCD process

- Designed a 12 V to 3.3 V, 1 A, 2 MHz synchronous (half-bridge) buck in Cadence Virtuoso using the TSMC 180 nm HV BCD PDK; optimized MOSFETs via width sweeps for loss/efficiency tradeoffs.
- Implemented gate driver with up/down level shifters, bootstrap, and dead-time; tuned edges and validated in ADE with 5.15% output ripple and 198 mA inductor ripple, verifying V_{GS}, level-shifter I/O, and bootstrap behavior.

Hybrid Converter PCB: 4-Layer Design in Altium

- Built a 4-layer hybrid-converter PCB from scratch in Altium: created custom symbol/footprint libraries, and generated Gerber and drill files.
- Applied EMI-aware stackup and layout, top/bottom partitioned for power and control; inner GND and VDD planes; minimized switching-loop and return paths with close decoupling and domain separation for signal and power integrity.

Teaching Experience

Graduate Teaching Assistant, University of Missouri - Columbia; UT Dallas — Fall 2024 – Present
Lecturer, Eastern University, Dhaka, Bangladesh — August 2023 – August 2024

Publications

- **M. Y. Rahman**, S. Singha, F. Makain, M. M. Hossain, and S. K. Islam, "A 1 MHz GaN-Based Transformerless Resonant Superimposed Quadratic Converter for 48 V-to-Point-of-Load High-Current AI Power Delivery," submitted to *CMOC* – 2026, under review.
- **M. Y. Rahman**, and S. M. Mominuzzaman, "Exploring Lead-Free Mixed Halide Double Perovskites Solar Cell," in *ICECE* – 2024, pp. 165–170. doi: 10.1109/ICECE64886.2024.11024609
- G. Taylor, **M. Y. Rahman**, M. M. Hossain, S. Singha, and S. K. Islam, "PDK-Accurate MOSFET Width Optimization for Efficient Integrated DC–DC Converters Using Spectre–MATLAB Co-Simulation," submitted to *DCAS* – 2026, under review.